MAXIMUM LIKELIHOOD BIT SYNCHRONIZER AND DATA DETECTOR

ABSTRACT OF THE DISCLOSURE

A bit synchronizer (16) that includes a tapped delay line (38) connected to a plurality of timing hypothesis circuits. A control and adjudication circuit (50) is connected to the timing hypothesis circuits, and compares outputs of the timing hypothesis circuits and selects one. Each of the timing hypothesis circuits includes a sum-and-dump summer (112) that is connected to outputs of the tapped delay line (38). The timing hypothesis circuits further include an absolute value circuit (46) and an averaging circuit (48). A select switch (60) is connected to the summers (112) and receives a switch control signal from the control and adjudication circuit (50). A threshold test circuit (62) compares the selected output signal to a threshold value and outputs a mark or space symbol.